REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1, 3, 4, 6-8, and 10-14 are now pending, claims 1, 4, 8, and 10 being independent. In this Reply, Applicant has amended claims 1, 4, 7, 8, and 10 and has canceled claims 2, 5, and 9 without prejudice or disclaimer.

Prior Art Rejection

Claims 1-14 stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over *Itoh et al.* (U.S. Patent 5,585,817) in view of *Ichikawa et al.* (U.S. Patent 6,127,998) and further in view of *Ueno* (U.S. Patent 6,496,224). This rejection is respectfully traversed.

The Claimed Invention

Independent claim 1 is directed to an image display apparatus generally comprising an imaging section and a display section. As amended herein, the imaging section recited in claim 1 is formed of a CCD imaging device for converting an optical image to first signals representing the image and includes: photoelectronic conversion devices arranged in the form of a matrix formed by lines and columns for converting the optical image to signal charges, vertical transfer paths arranged adjacent to the respective columns of the photoelectronic conversion devices, each of the vertical transfer paths transferring the signal charges toward one end in accordance with vertical driving pulses supplied from the outside,

transfer gates for transferring the signal charges generated by the photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses, and output circuits for converting signal charges arrived at the one end of the vertical transfer paths to signals and outputting the first signals in parallel column by column of the matrix, such that the imaging section outputs the first signals representing an image without horizontally transferring signal charges provided by said vertical transfer paths.

The display section recited in independent claim 1 includes: display devices arranged in the form of a matrix, input circuits, and a vertical driving circuit. The display devices each have a signal input terminal and a control signal input terminal, and display the image represented by the first signals applied to the image signal input terminal at the time of application of driving pulses to the control signal input terminal. The input circuits receive the first signals output from the imaging section in parallel column by column and output second signals corresponding the received first signals to the image signal input terminals over signal buses in parallel column by column of the matrix. The vertical driving circuit outputs the driving pulses to the control signal input terminals over control buses line by line of the matrix in a predetermined order.

Independent claim 1 specifies that the imaging section "outputs the first signals without horizontally transferring the signal charges provided by said vertical transfer paths." By providing an imaging section that outputs image signals from vertical transfer paths without requiring horizontal driving pulses, disclosed embodiments of the present invention are able to achieve reduced power consumption. (See e.g., p. 10, ll. 21-26 of the specification).

Independent claim 4 is directed to an image display apparatus comprising an imaging section (as substantially described above with regard to claim 1) and a display section, and further comprising a signal conversion section for processing the first signals output from the imaging section in parallel column by column and outputting processed signals as second signals in parallel. The input circuits for the display section recited in claim 4 receive the second signals from the signal conversion section in parallel and output third signals corresponding to the received second signals to signal input terminals over signal buses in parallel column by column.

Like independent claim 1, independent claim 4 specifies that output circuits convert signal charges arriving at one end of vertical transfer paths to the first signals and output the first signals in parallel column by column of the matrix, such that the imaging section "outputs the first signals without horizontally

transferring the signal charges provided by said vertical transfer paths."

Independent claim 8 is directed to an image display apparatus generally comprising an imaging section; a signal conversion section; and a parallel-to-serial conversion section. The imaging section of claim 8 is formed as a CCD device for converting an optical image to first signals representing the image and includes: photoelectronic conversion devices arranged in the form of a matrix formed by lines and columns for converting the optical image to signal charges; vertical transfer paths arranged adjacent to the respective columns of the photoelectronic conversion devices, each of the vertical transfer paths transferring signal charges toward one end in accordance with vertical driving pulses; transfer gates for transferring signal charges generated by the photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses; and output circuits for converting signal charges arrived at the one end of the vertical transfer paths to the first signals and outputting the first signals in parallel column by column of the matrix, such that the imaging section outputs the first signals without horizontally transferring the signal charges provided by the vertical transfer paths.

The signal conversion section of claim 8 processes the first signals output in parallel from the imaging section column by

column and outputs the processed signals as second signals in parallel, and the parallel-to-serial conversion section converts the second signals to serial signals.

Like independent claims 1 and 4, independent claim 8 specifies that the output circuits of the imaging section function such that the "imaging section outputs the first signals without horizontally transferring the signal charges provided by said vertical transfer paths."

Independent claim 10 is directed to a display apparatus comprising: a serial-to-parallel conversion section; a signal conversion section; and a display section. The serial-to-parallel conversion section converts first signals serially input thereto and representing an image to parallel second signals for output. The signal conversion section processes the second signals output in parallel from the serial-to-parallel conversion section column by column and outputs the processed signals as third signals in parallel. The display section includes: display devices arranged in the form of a matrix, each of the display devices having an image signal input terminal and a control signal input terminal, and displaying an image represented by third signals applied to the image signal input terminal at the time of application of driving pulses to the control signal input terminal; input circuits for receiving the third signals from the signal conversion section in parallel and outputting fourth signals corresponding to the

received third signals to the image signal input terminals over signal buses in parallel column by column of the matrix; and a vertical driving circuit for outputting the driving pulses to the control signal input terminals over control buses line by line of the matrix in a predetermined order.

The Asserted Grounds of Rejection/Deficiencies in the Rejection

In the Office Action dated May 21, 2003, the Examiner rejected all claims based on an asserted combination of *Itoh*, *Ichikawa*, and *Arakawa*. In this Office Action, the Examiner relies on *Ueno* as a secondary reference, instead of *Arakawa*. Applicant respectfully submits that the asserted combination of references fails to establish *prima facie* obviousness of any pending claim.

To establish *prima facie* obviousness, all claim limitations must be taught or suggested by the prior art and the asserted modification or combination of the prior art must be supported by some teaching, suggestion or motivation in the applied references or in knowledge generally available to one skilled in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The prior art must suggest the desirability of the modification in order to establish a *prima facie* case of obviousness. *In re Brouwer*, 77 F.3d 422, 425, 37 USPQ2d 1663, 1666 (Fed. Cir. 1995). It can also be said that the prior art must collectively suggest or point to the claimed invention to support the findings of obviousness. *In re*

Hedges, 783 F.2d 1038, 1041, 228 USPQ, 685, 687 (Fed. Cir. 1986); *In re Ehrreich*, 590 F.2d 902, 908-909, 200 USPQ 504, 510 (C.C.P.A. 1979).

In order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), the Examiner must provide particular findings as to why the two pieces of prior art are combinable. See *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). The issue of whether there is motivation to modify a reference must be based on the objective evidence of record, not subjective belief or unknown authority. *In re Lee*, 81 USPQ2d 1430 (Fed. Cir. 2002). Broad conclusionary statements standing alone are not "evidence." A modification of the primary reference that would change its principle of operation is contrary to a finding of *prima facie* obviousness. MPEP § 2143.01.

In this case, Applicant finds no objective evidence to support the conclusion that the prior art, or knowledge generally available to those of ordinary skill in the art, suggests a modification of *Itoh* that satisfies all the features of any pending claim. At least for this reason, the Office Action fails to establish *prima facie* obviousness.

Itoh discloses a combined image input/display apparatus that includes an image input section 20 and an image display section 10 with a data drive circuit 302, which is adapted to sequentially drive the columns of pixels, as seen in Fig. 3. Recognizing

differences between *Itoh* and the claimed invention, the Examiner relies on *Ichikawa* to conclude that:

> One would have been motivated in view of the suggestion in Ichikawa that the matrix inputting adjustment method in conjunction with serial--parallel conversion mechanism is functionally equivalent to the desired input an[d] output circuits configurations. The use of matrix inputting adjustment and serial-parallel conversion mechanism helps function liquid crystal display as taught by Ichikawa. (Office Action, pg. 3).

Furthermore, the Examiner relies on *Ueno* to conclude that:

> Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify Itoh's display image operation to adapt [sic] Ueno's technique of reading out signal charges from pixel columns along the vertical direction. One would have been motivated in view of the suggestion in Ueno that reading out signals from columns and vertical transferring as demonstrated in Fig. 4 equivalently provide the desired outputting from the output circuits and imaging section. The use of vertical transferring of charges helps function the process of imaging operation as taught by Ueno. (Office Action, pg. 4).

Therefore, the Examiner's rejection appears to be based on the conclusion that it would have been obvious to include a serial-parallel conversion element (from *Ichikawa*) and aspects of a CCD type imaging arrangement (from *Ueno*).

Initially, Applicant notes that the Examiner's reliance on serial-to-parallel conversion in *Ichikawa* is not relevant to the invention of independent claims 1, 4, and 8, which do not recite serial-to-parallel conversion.

Also, neither *Itoh* nor *Ichikawa* teach a CCD type of image sensor, as now more clearly recited in the pending claims. Although *Ueno*, as newly cited, teaches a CCD type of image sensor, *Ueno* merely teaches the thinning read out mode in which signal charges are read out in a CCD solid-state imaging device only from a portion of pixel columns in the vertical direction. (See e.g., Abstract). As such, *Ueno* fails to suggest a modification of *Itoh* as apparently relied on by the Examiner to reject the pending claims. It is also noted that the device taught by *Itoh* is not adapted to simultaneously drive both the image input section and the image display section of the apparatus described therein, as allowed with the Applicant's invention.

Therefore, even though *Ueno* teaches a CCD type image sensor, the asserted combination with *Itoh* and *Ichikawa* (assuming these references may be combined, which Applicant does not admit) fails to satisfy the features of Applicant's claims. It is therefore believed that the Applicant's claims are not rendered obvious by *Itoh*, even in view of *Ichikawa* and *Ueno*.

In addition to the above reasoning, Applicant submits that the stated grounds of rejection is deficient at least for the following reasons. The Examiner points out in the paragraph bridging pages 2 and 3 of the Office Action that *Ichikawa* teaches a matrix 803 in Fig. 23. It is important to note, however, that the matrix 803 of *Ichikawa* constitutes a key input device. By contrast, what is

referred to as a "matrix" in the claims is an array of photosensitive cells arranged in lines and columns in the imaging section as well as a corresponding array of display cells in the display section. An incorporation of the key matrix of the display cells taught by *Ichikawa* into the imaging section or the display section would not correspond to the matrix of lines and columns of the photoelectric conversion devices and display device recited in Applicant's claim 1, for example.

The Examiner also points out in the same paragraph that *Ichikawa* teaches a main board 453 from which an output is subjected to serial-to-parallel conversion. At least in terms of Applicant's independent claims 1, 4, and 8, the output circuits recited are adapted for converting the signal charges arriving at one end of the vertical transfer paths to image signals and forwarding the image signals to the display section in parallel column by column of the matrix. The Applicant's output circuits therefore do not read on the serial-to-parallel conversion included in the main board 453 of *Ichikawa*.

At least in view of the above, Applicant respectfully requests reconsideration and withdrawal of the Examiner's rejection under 35 U.S.C. § 103 based on the asserted combination of *Itoh*, *Ichikawa*, and *Ueno*.

Conclusion

Applicant respectfully requests that the Examiner enter the amendments presented herein, which are not believed to be of a nature that require further consideration and/or search by the Examiner.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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